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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/840,125	05/06/2004	Steve Ming Ting	TSM03-0945	7245
43859 7590 03/26/2008 SLATER & MATSUI, L.L.P. 17950 PRESTON ROAD, SUITE 1000 DALLAS, TX 75252			EXAMINER NADAV, ORI	
			ART UNIT 2811	PAPER NUMBER
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

**Application No.**

10/840,125

**Applicant(s)**

TING ET AL.

**Examiner**

Ori Nadav

**Art Unit**

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 January 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 16-33 is/are pending in the application.
- 4a) Of the above claim(s) 29-33 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 16-28 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 December 2006 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/S5108)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_
- Paper No(s)/Mail Date \_\_\_\_\_

### **DETAILED ACTION**

In view of the appeal brief filed on 1/10/2008, PROSECUTION IS HEREBY REOPENED. A new rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

### ***Specification***

The amendments filed 12/22/2006 and 4/24/2007 are objected to under 35 U.S.C. 132(a) because they introduce new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

1. In paragraph [0025], as amended 12/22/2006, the amendment "such that the notched spacer is thinner along the surface of the substrate, as illustrated in FIG. 1 j," is new matter.

Applicant is required to cancel the new matter in the reply to this Office Action.

***Drawings***

The drawings are objected to, because amended figures 1F, 1G, 1H, 1I and 1J, filed on 12/22/2006 and 4/24/2007, introduce new matter. For example, in figure 1j, spacer layers 132 having thinner regions along the side of the gate electrode and the gate dielectric is a new matter.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 16-28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There is no support in the specification as filed, for the claimed limitations of "a thickness of the notched spacer alongside the gate electrode is thinner near the substrate", as recited in claim 16, and for the claimed limitations of "removing at least a portion of the first layer along a surface of the substrate, thereby forming a notch in the notched spacer alongside the gate electrode near the substrate", as recited in claim 24.

There is no support in the disclosure and in the drawings for the claimed limitations of "performing a first ion implant wherein only the gate electrode and the notched spacer act as masks", as recited in claim 16.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 16-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitations of "a thickness of the notched spacer alongside the gate electrode is thinner near the substrate", as recited in claim 16, are unclear from which element the notched spacer alongside the gate electrode is thinner than.

The claimed limitations of "the etching process removing at least a portion of the first layer along a surface of the substrate", as recited in claim 24, are unclear as to how removing at least a portion of the first layer along a surface of the substrate relates to the etching process. It is further unclear as to which etching process applicant refers.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 16 and 23, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuegraf et al. (7,009,264) in view of Kinugawa (5,215,936). Regarding claims 16 and 23, Schuegraf et al. teach in figure 2D and related text a method of forming a semiconductor device, the method comprising:

forming a gate electrode 211 on a substrate, the substrate having a first conductivity type;

forming a notched spacer 221 alongside the gate electrode such that a thickness of the notched spacer alongside the gate electrode is thinner near the substrate, the notched spacer comprising a single silicon nitride homogenous layer;

Schuegraf et al. do not teach performing a first ion implant wherein only the gate electrode and the notched spacer act as masks during the first ion implant, the first ion implant using ions of the first conductivity type and performing one or more second ion implants using ions of a second conductivity type.

Kinugawa teaches in figure 3C and related text performing a first ion implant wherein only the gate electrode 15 and the spacer 17A act as masks during the first ion implant, the first ion implant using ions of the first conductivity type N in a substrate having a first conductivity type N.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to perform a first ion implant wherein only the gate electrode and the notched spacer act as masks during the first ion implant, wherein the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions of a second conductivity type in Schuegraf et al.'s device in order to operate the device in its intended use by simplifying the processing steps of making the device, and by using the device in a CMOS application (which requires first and second conductivity types implantations), respectively.

Claims 17-18, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuegraf et al. and Kinugawa, as applied to claim 16 above, and further in view of Chen et al. (6,610,571).

Schuegraf et al. and Kinugawa teach substantially the entire claimed structure, as applied to claim 16 above, except teaching the method of forming the notched spacer. Chen et al. teach in figures 2-3 and related text a method of forming a spacer comprises forming a first layer 50 and a second layer 52, forming a mask out of the second layer on the first layer such that the first layer alongside the gate electrode is covered by the mask, etching the first layer 50 such that the first layer 50 along a surface of the substrate 10 next to the gate electrode 14 is removed, and removing the mask (the portion of layer 52, as depicted in figure 4, which was used as a mask). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form prior art's spacer by forming a first layer and a second layer, forming a mask out of the second layer on the first layer such that the first layer alongside the gate electrode is covered by the mask, etching the first layer such that the first layer along a surface of the substrate next to the gate electrode is removed, and removing the mask, in order to simplify the processing steps of making the device by using a conventional method.

Claims 16 and 22, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Singh et al. (6,417,084) in view of Kinugawa (5,215,936).

Regarding claims 16 and 22, Singh et al. teach in figures 6-11 and related text a method of forming a semiconductor device, the method comprising:

forming a gate electrode 70 on a substrate, the substrate 62 having a first conductivity type;

forming a notched spacer 74 alongside the gate electrode such that a thickness of the notched spacer alongside the gate electrode is thinner near the substrate, the notched spacer comprising a single silicon dioxide homogenous layer;

Singh et al. do not teach performing a first ion implant wherein only the gate electrode and the notched spacer act as masks during the first ion implant, the first ion implant using ions of the first conductivity type and performing one or more second ion implants using ions of a second conductivity type.

Kinugawa teaches in figure 3C and related text performing a first ion implant wherein only the gate electrode 15 and the spacer 17A act as masks during the first ion implant, the first ion implant using ions of the first conductivity type N in a substrate having a first conductivity type N.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to perform a first ion implant wherein only the gate electrode and the notched spacer act as masks during the first ion implant, wherein the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions of a second conductivity type in Singh et al.'s device in order to operate the device in its intended use by simplifying the processing steps of making the

device, and by using the device in a CMOS application (which requires first and second conductivity types implantations), respectively.

Claims 17 and 19, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Singh et al. and Kinugawa, as applied to claim 16 above, and further in view of Chen et al. (6,610,571).

Singh et al. and Kinugawa teach substantially the entire claimed structure, as applied to claim 16 above, except teaching the method of forming the notched spacer.

Chen et al. teach in figures 2-3 and related text a method of forming a spacer comprises forming a first layer 50 and a second layer 52, forming a mask out of the second layer on the first layer such that the first layer alongside the gate electrode is covered by the mask, etching the first layer 50 such that the first layer 50 along a surface of the substrate 10 next to the gate electrode 14 is removed, and removing the mask (the portion of layer 52, as depicted in figure 4, which was used as a mask).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form prior art's spacer by forming a first layer and a second layer, forming a mask out of the second layer on the first layer such that the first layer alongside the gate electrode is covered by the mask, etching the first layer such that the first layer along a surface of the substrate next to the gate electrode is removed, and removing the mask, in order to simplify the processing steps of making the device by using a conventional method.

Claims 20-21, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuegraf et al. and Kinugawa, or over Singh et al. and Kinugawa, as applied to claim 16 above, and further in view of Applicant Admitted Prior Art (AAPA). Singh et al. and Kinugawa, and Singh et al. and Kinugawa, separately teach substantially the entire claimed structure, as applied to claim 16 above, including impurities of the first conductivity type are implanted in the substrate below the gate electrode.

Prior art does not state that the step of performing a first ion implant is performed by implanting ions at an oblique angle to the substrate and the step of performing one or more second ion implants is performed at an angle normal to a surface of the substrate. AAPA teaches in paragraphs [0004] to [0007] implanting ions at an oblique angle to the substrate and at an angle normal to a surface of the substrate.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form prior art's first ion implant by implanting ions at an oblique angle to the substrate and the step of performing one or more second ion implants is performed at an angle normal to a surface of the substrate, in order to obtain proper doping distribution.

Claims 24 and 27-28, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Kinugawa. Regarding claims 24 and 27-28, Chen et al. teach in figures 2-10 and related text a method of forming a method of forming a semiconductor device, the method comprising:

forming a gate electrode 14 on a substrate 10, the substrate having a first conductivity type;

forming a first layer 50 of silicon oxide over the substrate and the gate electrode;

forming a second layer 52 of silicon nitride over the first layer;

removing a portion of the second layer such that a spacer mask 52 (figure 3) is formed on the first layer on a side of the gate electrode;

etching the first layer to form a notched spacer 50 (figure 4) wherein the spacer mask acts as a mask,

the etching process removing at least a portion of the first layer along a surface of the substrate, thereby forming a notch in the notched spacer alongside the gate electrode near the substrate;

removing the spacer mask (the portion of layer 52, as depicted in figure 4, which was used as a mask);

Chen et al. do not state that a first ion implant is performed after the spacer mask has been removed, wherein the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions of a second conductivity type.

Kinugawa teaches in figure 3C and related text performing a first ion implant wherein the first ion implant using ions of the first conductivity type N in a substrate having a first conductivity type N.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to perform a first ion implant wherein the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions

of a second conductivity type in Chen et al.'s device in order to operate the device in its intended use by simplifying the processing steps of making the device, and by using the device in a CMOS application (which requires first and second conductivity types implantations), respectively.

Claims 25-26, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. and Kinugawa, as applied to claim 24 above, and further in view of Applicant Admitted Prior Art (AAPA).

Chen et al. and Kinugawa teach substantially the entire claimed structure, as applied to claim 24 above, including impurities of the first conductivity type are implanted in the substrate below the gate electrode.

Prior art does not state that the step of performing a first ion implant is performed by implanting ions at an oblique angle to the substrate and the step of performing one or more second ion implants is performed at an angle normal to a surface of the substrate. AAPA teaches in paragraphs [0004] to [0007] implanting ions at an oblique angle to the substrate and at an angle normal to a surface of the substrate.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form prior art's first ion implant by implanting ions at an oblique angle to the substrate and the step of performing one or more second ion implants is performed at an angle normal to a surface of the substrate, in order to obtain proper doping distribution.

***Response to Arguments***

Applicant's arguments were adequately addressed in previous office action.

The rest of applicant's arguments with respect to claims 16-28 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References E-L are cited as being related to notched spacers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For

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more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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3/29/2008

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